ABSTRACT
A Precision Time-Frequency Estimator (PTFE) method for measuring clock time and frequency differences among multiple distributed devices connected by conventional low-bandwidth interfaces is proposed. The clocks being compared may have different frequencies. Picosecond-level timing accuracy is achieved by tracking the phase of a beat signal created by digitally mixing the two clock signals. Clock cycle ambiguity is resolved by using reference event pulses from the two clocks to relate the beat signal phase to the reference event pulses. The PTFE implementation requires minimal hardware resources and pairs of PTFE instantiations may be used to determine cable delays for synchronization between distributed devices. The performance of the proposed approach is demonstrated with results from laboratory testing.

INTRODUCTION
In federated architectures, individual sensors and devices are often clocked independently because their designs are optimized and matured separately in their development. As modern systems become more highly integrated, there is an increasing need for information fusion of data that originates from these federated sensors/devices that require tight timing synchronization and frequency syntonization. For sensors that involve RF ranging/timing, navigation-level timing synchronization is needed at a precision of 1 ns or less. In signal intelligence (SIGINT) applications, the coordination of frequency (or syntonization) is often of equal or greater interest and generally requires a precision on the order of 0.1 ppb or less.

An illustration of a potential application for such time/frequency coordination is shown in Figure 1. Here a SIGINT platform with one or more sensor payloads requires accurate time and frequency references. This need becomes even more pronounced when data from multiple platforms are combined. Stable frequency can be obtained from an Atomic Frequency Standard (AFS) and GPS can provide an absolute time reference (i.e., synchronized to UTC). However if there are multiple sensors and communication systems on the platform then some way of distributing the stable AFS frequency is needed. It is not always practical to collocate sensors, radios, and other devices, so often each sensor will have a GPS receiver and/or AFS, yielding increased cost, suboptimal implementations, and logistical problems. Furthermore, frequency standards on radios and sensors are often chosen to optimize the frequency plan for each individual device application and so time/frequency coordination across heterogeneous clock frequencies is desirable.

As depicted in Figure 1, we propose to solve the problem of time-frequency distribution through a Precision Time-Frequency Interface (PTFI) which operates over standard low-bandwidth copper cabling. Each PTFI employs one or more PTFE circuits which compare clock and reference time pulses from pairs of devices to determine the time and frequency offsets between the devices. The PTFE
outputs the time and frequency differences as digital data, which enables creation of one or more “paper clocks” for the platform. This timing data can then be incorporated into centralized Positioning, Navigation and Timing (PNT) processing on the platform which can then provide optimal time reference data for all platform applications.

This paper is organized as follows: first other methods for time-frequency coordination are reviewed and their shortcomings described; next a description of the PTFE operation is presented along with performance tradeoffs; next sample laboratory results are shown, indicating synchronization at the 10 ps-level is achieved; and finally it is shown how multiple PTFEs can be utilized to create a PTFI where cable delays can be tracked to maintain synchronization of distributed devices over time.

**REVIEW OF TIME-FREQUENCY COORDINATION TECHNOLOGIES**

The most common approach to synchronization is the Time Interval Counter (TIC), which is used to accurately measure the time difference between two events defined by pulses from two independent sources [1]. These pulses, each of which defines the timing of its sensor source and are typically derived from a clock pulse, must be shaped with very sharp edges and transported with broadband cabling to ensure the high frequencies that defined those sharp edges are preserved. The high frequency content needed to maintain the sharp pulse edges extend considerably higher than the clock’s intrinsic frequency itself.

The resolution of the TIC is determined by the local oscillator frequency and stability. To prevent ambiguity in the identification of the pulses, they are typically transmitted at a relatively low rate, for example once every second, allowing time for digital communication messages between the two systems to clearly identify each pulse with respect to each system’s local time reference. If pulses are transmitted too frequently, ambiguity could arise in pulse identification.

The limit of the integer resolution of the local clock used to time the interval between the two pulses generally requires the sampling frequency be high for precise relative timing. To mitigate the need for high frequency references, for example 20 ps would require 50 GHz, interpolation techniques are employed. Interpolation allows fractional clock cycle counting which increases resolution beyond the local oscillator clock. Time-to-Digital-Converter (TDC) techniques can be implemented on a low-cost FPGA (field programmable gate array). The Vernier method, for example, can achieve < 100 ps uncertainty. Fully digital systems typically achieve 50-500 ps [2]. However, a TDC is limited to providing time difference information between input clocks, and does not provide frequency difference information. TDC methods also increase implementation complexity.

TIC measurements require the pulse edges to be well defined and low in noise and jitter, because these effects could cause inaccurate triggering of the counter start or stop times. Because of the need to limit the rate of pulses for disambiguation, the number of time intervals measured per rate of time is kept low, so it takes a significant amount of time to average out any sampling errors due to pulse edge jitter and noise. In systems that can tolerate long initialization times and have very stable clocks, such as calibrating a precision ground based atomic clock using a pulse per second from a GPS receiver, long averaging times to reduce error can be tolerated. However, for systems that must be synchronized quickly, or that use lower cost clocks that drift at a higher rate, these long averaging times are unacceptable and result in reduced relative timing accuracy.

Another synchronization concept, less widely-used than TICs, is the Dual Mixer Time Difference (DMTD) [5]. In the DMTD, the phase difference of two input clock signals (Osc. #1 and Osc. #2) at the same nominal frequency is determined by mixing the two input clock signals with an internally-generated clock signal (Xfer Osc.), whose frequency is a few Hz off from the input signals. The outputs of the two mixers (ν₁−ν₀) and (ν₂−ν₀) are also nominally the same frequency as each other but at a much lower frequency than the two input clock signals. At this lower frequency the time interval counter may be used to measure the relative timing of the outputs of the two mixers to deduce the relative phase of the signals.

**Figure 2. Dual Mixer Time Difference (DMTD) System (from paper by D. Allan et al, [5])**

A digital implementation of the DMTD, known as the Digital Dual Mixer Time Difference (DDMTD) [4] performs a similar function. By sampling, deglitching and counting the intervals between the two sampled outputs, the relative phase of two input clocks of very similar or equal frequencies may be determined, as depicted in Figure 3.

The White Rabbit (WR) system at CERN is typical of systems utilizing the DDMTD. Before the DDMTD phase offset calculation may be performed, the clocks in WR at two points must be syntonized (made equal in
frequency) via digital phase lock loops (DPLLs). All clocks are slaved to a single master clock. This is accomplished via SyncE protocol using DPLLs.

Once all the clocks in the system have been synchronized, the WR system calculates cable delay from coarse offsets using time-tagged two-way messaging, and fine phase offset measurements using the DDMTD method. These phase offsets are used to adjust the slave clock so that it matches the master clock. The system is then periodically checked. The WR system utilizes very stable clocks and takes advantage of the fact that the phase offsets are relatively fixed during the measurement period. This allows the phase resolution to be enhanced. Phase drift is expected to be caused by temperature and occurs slowly allowing updates rates as low as one adjustment per hour.

Although the DMTD and DDMTD work well in controlled experimental environments in which stable clocks of common frequencies may be utilized, and the cost of precision clocks and additional DPLL hardware is not a significant concern, in many applications such as aircraft, ground vehicles, ships, and remote or mobile ground installations, clock frequencies of various sensors may not be similar. In addition, these applications may be very sensitive to the cost of added hardware and may not be able to tolerate syntonization of the clocks in the various sensors and processing systems.

PTFE OVERVIEW

In contrast to the TIC and DMTD, the PTFE/PTFI tackles the problems of synchronization and syntonization simultaneously with a novel approach that also redefines the timing interfaces involved. Instead of defining the timing of each sensor with infrequent pulses, we instead define it with clock signals and event pulses. The relative frequency and phase between two clock signals is determined and the event pulses from each source are used to resolve the integer ambiguity as to which cycle of each clock is associated with a given absolute time or system time mark. In this way, the need for a maintaining a sharp low noise and jitter edge of the pulse event goes away.

The PTFE uses a clock signal that provides many more edges or phase transitions per unit of time, dramatically reducing the time required to average out any noise and jitter on the clock lines and eliminating the need for very sharp low-noise timing pulses between systems.

This approach has several benefits:

- The bandwidth demands of generating and transporting the event pulses and clock signals are lower than those required in the conventional approach, i.e., RF frequencies such as 10 MHz vs. very fast optical pulses;
- Timing synchronization and frequency syntonization can be simultaneously determined and tracked in real time with extremely high precision, creating a virtual clock at each sensor tracking the difference with other sensor clocks;
- Fast real-time tracking of the relative clock phase and frequency also allows these low-cost quartz clocks to be continuously calibrated with respect to a highly-stable clock for all system timing to derive the benefit of that highly-stable clock;
- This approach can be efficiently implemented digitally and hosted on compact devices or on processors shared with other functions;
- Ease of replicating the PTFE function allows multiple uses within a federated architecture.

Figure 4 shows a typical application of the PTFE. A first sensor (Sensor A) generates a reference clock at frequency F_A and a disambiguation event pulse at periodic times T_A. A second sensor (Sensor B) generates a reference clock at frequency F_B and a disambiguation event pulse at periodic times T_B. Note that the PTFE system may be packaged with either or both of the two sensors, or remotely mounted from both. PTFE generates a precise measurement of the relative frequencies of the clocks (F_A and F_B) as well as a time difference between the two sensors consisting of both a number of integer clock cycles (such as the number of cycles of F_A occurring between T_A and T_B) and the relative phase between the two clocks (such as the phase or portion of a cycle of F_A that F_B is ahead or behind F_A at the current cycle, or clock edge, of F_A).
PTFE IMPLEMENTATION

The PTFE is an all-digital method for measuring relative frequency and relative timing between two input clocks. The input clock frequencies can be dissimilar, and can also be phase incoherent. The method uses short-term averaging to produce time and frequency difference estimates. A block diagram for the system is shown in Figure 5.

Frequency Measurement

The PTFE circuit first samples the clock inputs with flip-flops to produce a clock signal whose frequency is the difference between the two clocks, $F_{\text{DIFF}} = F_A - F_B$. Note that the single sampling flip flops, shown Figure 5, are implemented as a pair of cascaded flip-flops to prevent meta-stability issues. The edges from the $F_{\text{DIFF}}$ clock signal are compared against a clock generated from a Numerically Controlled Oscillator (NCO). The NCO can be initialized with a rate if the clock frequencies are known beforehand. The NCO rate does not need to be exact, since the NCO clock rate will converge quickly to $F_{\text{DIFF}}$. If the input clock frequencies are unknown, a counter circuit can be added to determine the clock frequencies and set an initial NCO rate. The results of the edge comparison are sent to an accumulator which accumulates over a set period (typically 1 ms). The accumulator is sent either a -1, 0, or +1 at every $F_A$ clock cycle, depending on the relationship of the $F_{\text{DIFF}}$ clock edge to the NCO clock edge. For example, if the NCO predicts a transition from high to low two Clock A signal samples before the Clock B signal $(fA - fB)$, then the edge compare will output a total comparison of 2 (it will output a plus one signal twice). The accumulated values are then sent to a Control Filter Servo implemented as a Proportional-Integral (PI) Controller Loop, which adjusts the NCO rate, and the accumulator is reset. The PTFE outputs the NCO rate as digital data. The NCO measurement can occur as often as every accumulator cycle, or longer, depending on the communication interface and frequency and time difference update rate requirements (e.g., serial, Ethernet).

For our applications, the NCO width was chosen to be 40 bits to achieve single picosecond timing resolution. One specific application we are pursuing is synchronizing a Rockwell Collins SAASM GPS receiver, with a frequency reference with a nominal frequency of 10.949187 MHz, with a 10 MHz AFS. With a 40-bit NCO, the least significant bit (LSB) gives a frequency resolution of approximately $10^{-5}$ Hz, which is approximately 1 part per trillion. This LSB frequency resolution equates to a difference in period between a 10 MHz signal, and 10 MHz + 1 LSB signal, of approximately $10^{19}$ seconds. Over a 1 ms measurement

![Figure 5 PTFE Implementation including time mark event signals](image-url)
period, the accumulated period error for a 1 LSB NCO error is $10^{-16}$. The clock frequency $F_B$ is determined with respect to $F_A$ as

$$F_B = \frac{1}{T_B} = \frac{F_A}{1 - \text{NCO RATE}} \quad (1)$$

Where NCO_RATE is the current value for the NCO step rate. This value is adjusted based upon Control Servo Filter output. The PTFE operation works best when the relative phase between clocks A and B varies significantly over the integration period.

**Time Measurement**

The PPS signals from each system identify specific clock edges to be used to determine the current relative time between the two systems ($T_{\text{DIFF}}$). The integer part of the time difference is obtained by counting the $F_A$ clock periods between the two PPS pulses. Figure 6 shows the relationship between clock edges to estimate time difference. PPS can be external (or internally derived) 1 PPS for each clock, or other time mark chosen for the system. The interval should vary enough from the input clocks to avoid ambiguity.

**Frequency Estimation**

The frequency estimation results shown in Table 1 were obtained using a SRS PRS-10 Rubidium for $F_A = 10$ MHz, and a signal generator set at $F_B = 10.949187$ MHz. The signal generator is phase locked to the 10 MHz output from the PRS-10 in order to expedite data analysis. The PTFE does not require phase locking for any clocks for proper operation. The statistics in the table below represent approximately 3600 measurements collected once per second for an hour. Each one-second measurement represents the average NCO value over the previous 512 ms (512 PTFE update cycles). Cable biases were not removed from the data sets. Standard Deviation is used as the measurement for repeatability and resolution range.

**LAB RESULTS**

Prototype testing was done at Rockwell Collins in the Advanced Technology Center laboratory. The PTFE is small footprint VHDL, and as such more than one PTFE can easily be instantiated on a single FPGA, and/or run alongside other resident code, such as waveform processing. The clocks in the lab testing were external, but internal Local Oscillators (LO) may also be fed to the circuit.

The following equipment was used to measure PTFE performance:

- Altera Cyclone III FPGA (can host multiple PTFEs on-board)
- SRS PRS-10 Rubidium, 10.0 MHz
- Symmetricom (Microsemi) CSAC SA-45, 10.0 MHz
- Agilent Function Generator, 10.949187 MHz
- Sine wave to TTL converter (in-house)

The PRS-10 and CSAC SA.45 were used in different tests as the reference clock, which allowed us to compare results with different reference clock characteristics.

![Figure 7 Block diagram of test equipment for PTFE validation test with Keysight TIC](image-url)

**Table 1 Frequency Results**

<table>
<thead>
<tr>
<th>Statistic</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>min</td>
<td>10949187.499201 Hz</td>
</tr>
<tr>
<td>max</td>
<td>10949187.500869 Hz</td>
</tr>
<tr>
<td>range</td>
<td>1.848200336 mHz</td>
</tr>
<tr>
<td>average</td>
<td>10949187.500004 Hz</td>
</tr>
<tr>
<td>std dev</td>
<td>0.287 mHz</td>
</tr>
<tr>
<td>bias</td>
<td>-3.772E-06 Hz</td>
</tr>
</tbody>
</table>
Precise Time Interval

The PTFE time difference estimates were evaluated with a Keysight 53230A TIC with resolution of 20 ps that was setup to report time measurements simultaneously with the PTFE operation. The aggregated results for several hour long tests are shown in Table 2. Cable biases were not removed from the data sets. Standard Deviation is used as the measurement for repeatability and resolution.

<table>
<thead>
<tr>
<th>Table 2 Time Interval Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTFE (&lt;10 ps resolution)</td>
</tr>
<tr>
<td>Min (ms)</td>
</tr>
<tr>
<td>Max (ms)</td>
</tr>
<tr>
<td>Average (ms)</td>
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<tr>
<td>Std Dev (ns)</td>
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<tr>
<td>Bias (ns)</td>
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</table>

Clock Jitter

Measurements of the clocks used in lab testing shows they have jitter in the 20-80 ps range, as shown in Figure 8 and Figure 9. While use of the TIC and the lab clocks were sufficient for initial prototype validation, they were clearly inadequate for evaluating PTFE performance limits. Next steps in testing will be replacing the atomic input clocks with a more stable 10 MHz OXCO, or Cesium source, depending on availability. Additionally, an independent method to verify the PTFE reports, with better than 20 ps accuracy obtained from the Keysight TIC, is needed.

PRECISION TIME-FREQUENCY INTERFACE WITH DUAL PTFE

A PTFI can be constructed from multiple PTFEs that can determine the relative time between two sensors or systems with independent clocks even if the cable length and propagation delay is not known. As shown in Figure 10, in this application two subsystems or sensors are each connected to a PTFE module and the clocks and time mark signals are fed in both directions between the two systems. From the two PTFE measurements both the relative time of the two sensors and the cable delay may be determined.

Note that in the figure we show the two paths as separate lines. This bidirectional communications may be implemented, for example, as a single cable bundle with two sets of twisted shielded pairs or two coaxial or fiber optic cables of the same length, each carrying a signal in one direction. However, the signals may also be multiplexed into one copper cable or fiber optic cable. The fast measurements of the PTFE enable time domain multiplexing of the signals, and the fact that the PTFE only requires relatively low data bandwidth on its clock and time mark event signal allow these signals to be
modulated onto higher frequencies that could be frequency division multiplexed in opposite directions on the same coaxial cable. The low data rate required also enables the use of low cost, low modulation rate LED or laser diodes. Different wavelengths could be used in different directions to reduce problems of back reflections. However the fact that PTFE effectively averages many measurements of clock edges make it less susceptible to interference from back reflections, so in some applications (especially when back reflections at each end may be minimized) the same RF frequency or optical wavelength may be used in both directions.

**SUMMARY**

The PTFE concept introduced here extends state of the art timing techniques to a much wider range of applications by eliminating the need to synchronize remote clocks, accommodating more rapid variation in relative clock frequency, and eliminating the need for high bandwidth timing signals between systems. In particular the PTFE works with timing sources that operate at different frequencies and the concept can be extended to work over unknown cable delays. The PTFE technique has been demonstrated to provide 10 ps-level relative timing, although the ultimate performance remains to be verified, pending testing with improved instrumentation. The PTFI holds the promise of providing a means for improved synchronization of sensors, enabling significant advancements in performance for a variety of aviation, navigation, and communication applications.

**REFERENCES**